

Tuesday, December 1st, 2026

Time	Titles	Speakers or additional info
08:15-08:30	Registration	
08:30-08:40	Welcome / Introduction	Knut Båttstøløkken
08:40-09:40	KeyNote Session	<i>Chairman: Knut Båttstøløkken</i>
08:40-09:40	How cybersecurity and the CRA will change your job as a test engineer	Steve Summers, Emerson Test and Measurement (NI)
09:40-10:20	Exhibitor Forum: short presentations	<i>Chairman: Artur Jutman</i>
10:20-11:00	Coffee Break / Exhibition	
11:00-12:30	Session 1: Structural test 1 / Test strategies	<i>Chairman: Mika Pussinen</i>
11:00-11:30	1.1 The Evolution of Testing: How AI empowers Test Program Generation	Lothar Diez, SPEA
11:30-12:00	1.2 ULTRA technology: A must to meet hyperscale's test needs	Andrea Romano, Seica
12:00-12:30	1.3 From DFT to Production Confidence: Practical Strategies for Modular, High-Coverage Electronics Test	Vojtech Camfrla, UNITES Systems a.s.
12:30-13:30	Lunch	
13:30-15:00	Session 2: Structural test 2 / Test Automation	<i>Chairman: Paulius Musteikis</i>
13:30-14:00	2.1 Faster inspection with deeper insight & Intelligent verification station	Chanderkant Vaid, GÖPEL electronic GmbH
14:00-14:30	2.2 Next level thermal imaging for detecting open ends for non-destructive validation testing	Dirk Faber, CN Rood
14:30-15:00	2.3 The Next Test Bottleneck: Scaling Electronics Production Without Scaling Labor	Dragos-Andrei Beldiman, Brooks
15:00-15:40	Coffee Break / Exhibition	
15:40-17:10	Session 3: IJTAG / Security	<i>Chairman: Raimedas Sodaitis</i>
15:40-16:10	3.1 IJTAG in Practice: Where Interoperability Still Breaks, and What Is Being Done About It	Reginald Waller, Asset Intertech
16:10-16:40	3.2 Security Challenges in Design-for-Test Across the Silicon Lifecycle	Erik Larsson, Lund University
16:40-17:10	3.3 The evolution of CAD formats in the electronics industry	Hermann Reischer, Polar Instruments GmbH
17:10-17:40	Fruit & Refreshments / Exhibition	
17:40-19:00	Panel debate:	<i>Panel moderator: Birger Schneider</i>
	Cybersecurity, Cyber Resilience Act (CRA) and Other Security Issues in Testing of Electronics	
19:30	Gala Dinner	

Wednesday, December 2nd, 2026

Time	Titles	Speakers or additional info
08:30-10:00	Session 4: Test data analysis	<i>Chairman: Erik Larsson</i>
08:30-09:00	4.1 Test data analysis with WATS Alvea and MCP	Natanya Sukkot, Virinco
09:00-09:30	4.2 Finding the Signal in the Noise: Hidden Insights from Manufacturing Test Data	Yee Shuen Hung, Keysight Technologies
09:30-10:00	4.3 PCB Repair and Rework with AI That Knows the Board and Its History	Giorgio Insinga, ARBoard
10:00-10:45	Coffee Break / Exhibition	
10:45-12:15	Session 5: JTAG based test / RF test	<i>Chairman: Mattias Ericsson</i>
10:45-11:15	5.1 Embedded ISP in combination with JTAG Embedded Test	Jan Heiber, Göpel electronic
11:15-11:45	5.2 Using Freely available libraries and tools to enhance JTAG Functional Test	Anthony Sparks, JTAG Technologies
11:45-12:15	5.3 From Model to RF: Practical Prototyping and Validation for Next-Generation Wireless Systems	Aku Wilenius, CN Rood
12:15-13:30	Lunch	
13:30-15:00	Session 6: AI	<i>Chairman: Mats Klarholm</i>
13:30-14:00	6.1 Why AI is Becoming Essential in Test—and How Nigel Enables It	Steve Summers, Emerson Test and Measurement (NI)
14:00-14:30	6.2 Accelerating Test Development with AI: Keysight's Open Tap Approach and Vision	Xavier Lory, Keysight
14:30-14:45	Short break	
14:45-15:45	Session 7: Functional test /	<i>Chairman: Harri Korhonen</i>
14:45-15:15	7.1 AI engineered functional test: Agent-controlled instrumentation with MCP interface	Artur Jutman, Testonica
15:15-15:45	7.2 Testblox, A new integrated in-fixture instrumentation platform for automated functional test	Bo Öhrwall, CEO Testblox AB
15:45-16:00	Closing Session: TestForum concluding remarks	<i>Knut Båtstøløyken, Kitron</i>

Technical Program for TestForum 2026

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