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New and Emerging JTAG Standards:

Changing the Paradigm of Board Test

(*A tutorial*)

Artur Jutman

NTF
NORDIC TEST FORUM

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Drammen, NORWAY

Presentation Outline

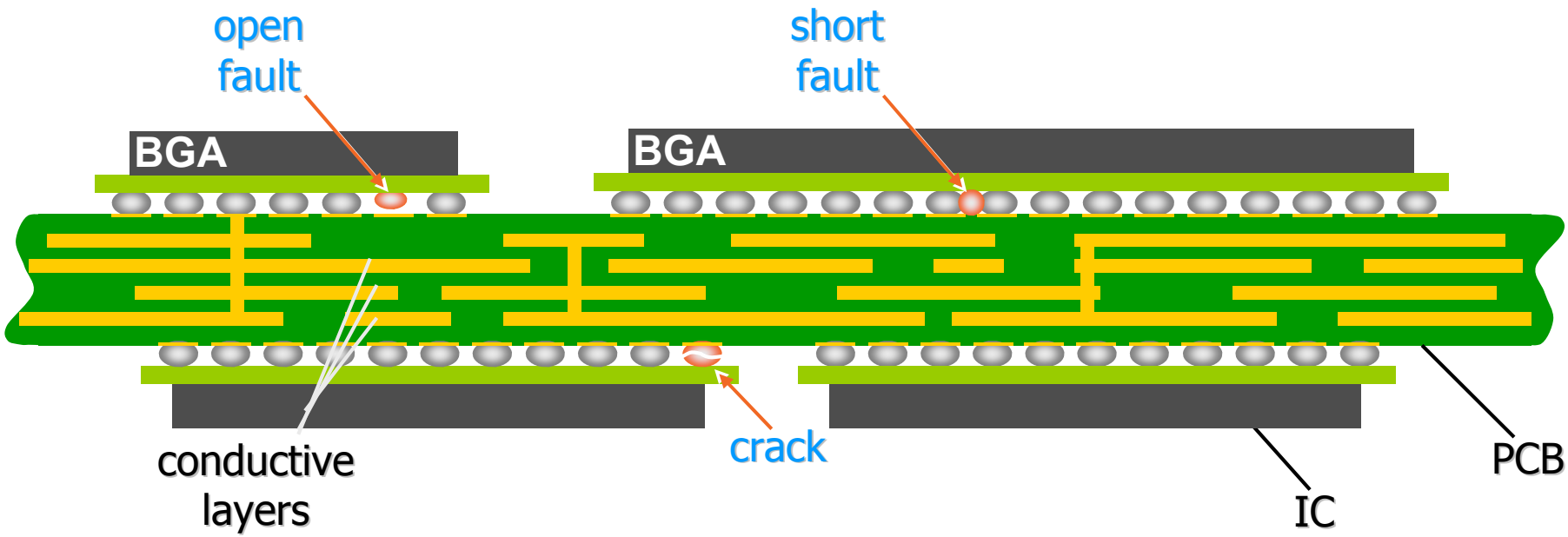
- Introduction
- Overview of the standards
- IEEE 1149.7
- IEEE P1149.1-2011
- IEEE P1149.8.1
- IEEE P1687
- Conclusions & Discussion

What's up!?

- The world went crazy…
- IJTAG
- SJTAG
- cJTAG
- CJTAG
- dot7
- dot8.1
- dot1-2011
- what's the reason?

The test access problem…

Limited access (nail probing) for test, measurement, diagnostics



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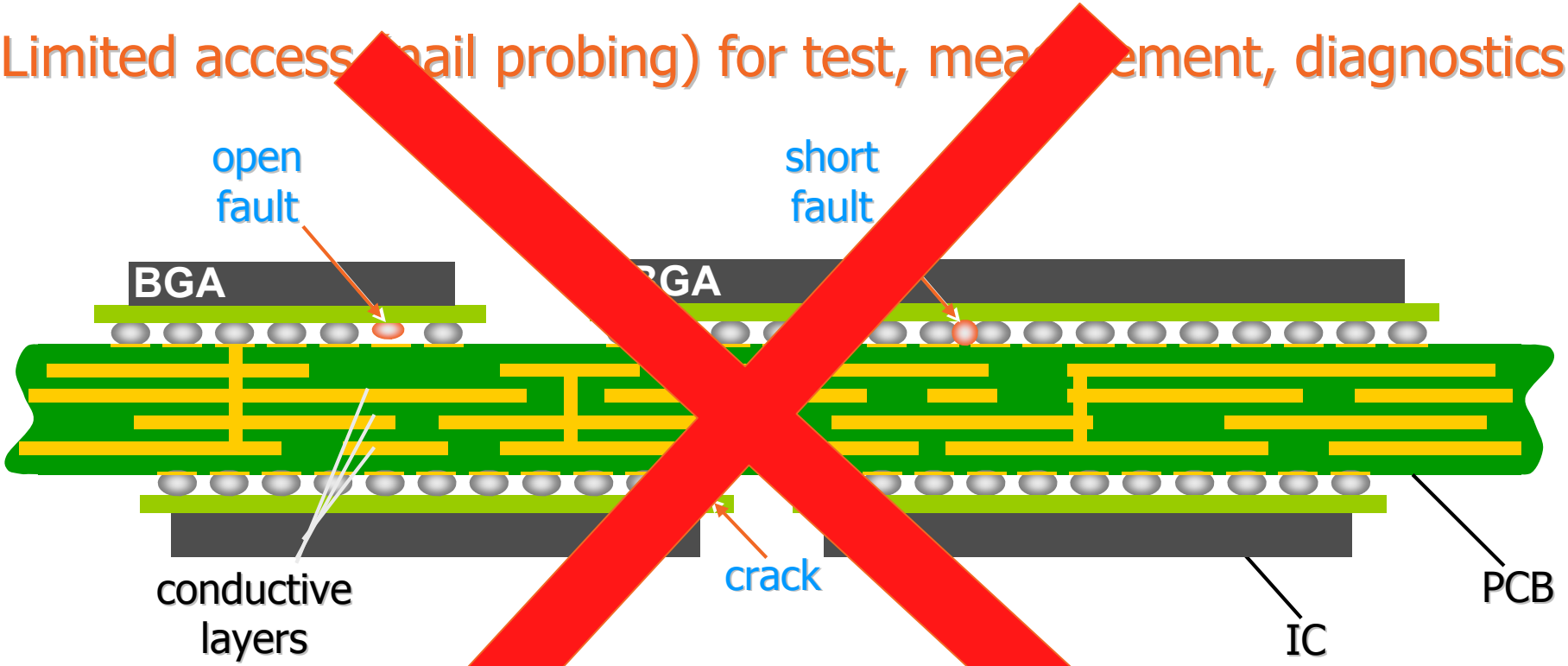


Such a slide is traditionally shown when introducing the Boundary Scan…

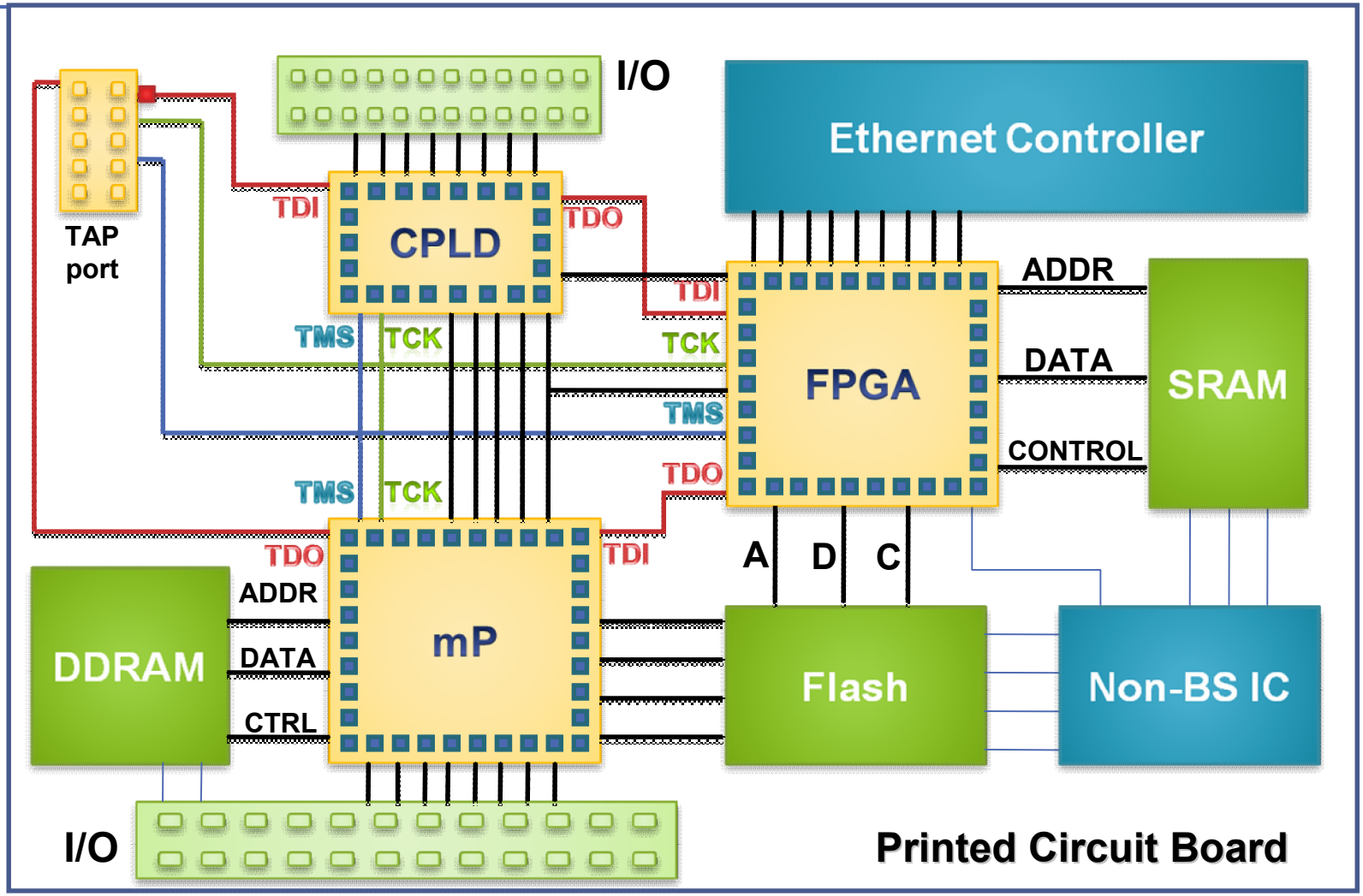
… already for more than 20 years!!!

"…BGA…"

"Test access is a problem"

"…bed of nails…"

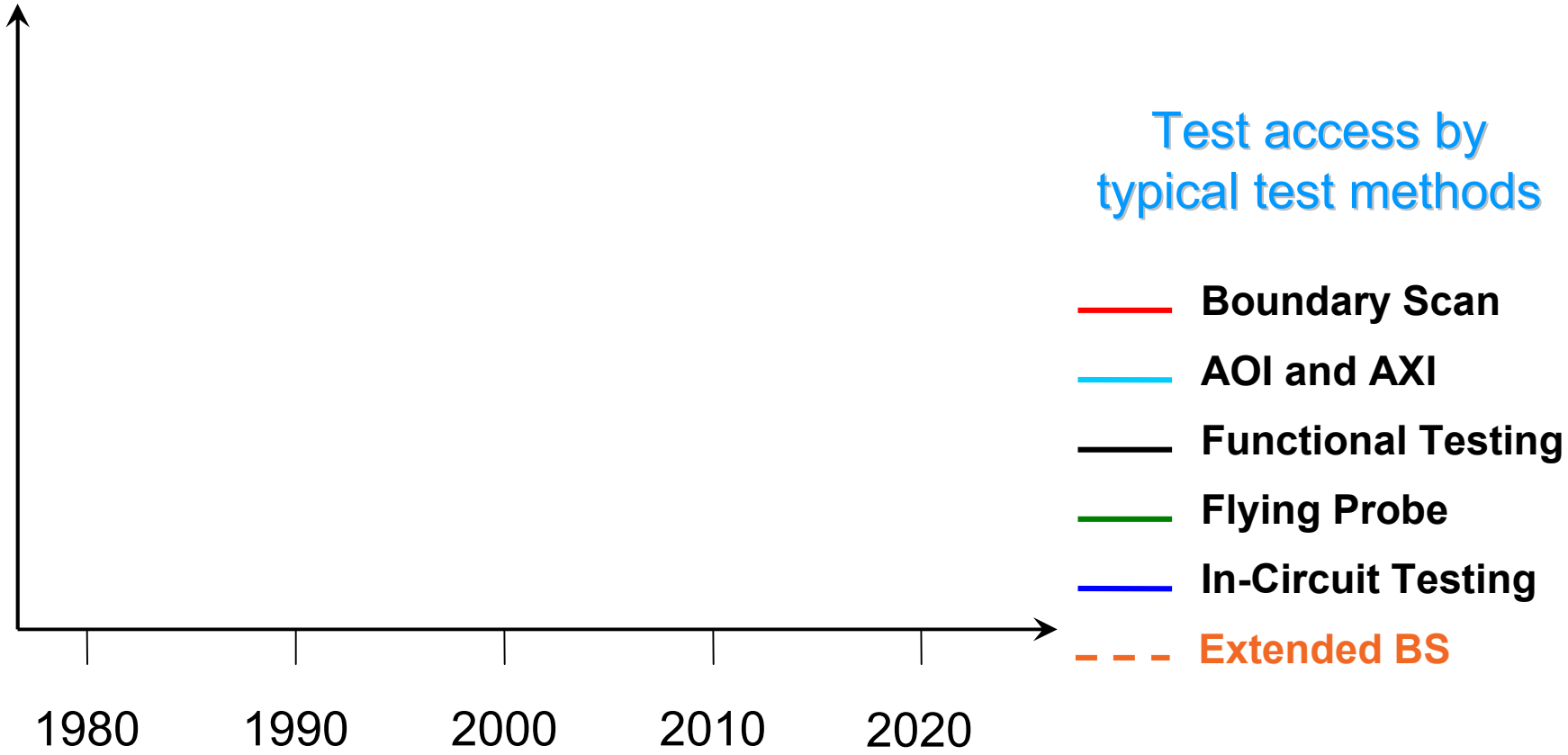
Test Access Via Boundary Scan



Typical case: the more BGAs on board, the better the test access

Test Access: Past and Present

- Past: test access was a problem
- Present: good test access by Boundary Scan combined with AOI, Functional Test, Flying Probe, etc.



Test Access: The Near Future

- Test access is not a problem due to extensive usage of DFT standards and rules
- But there are new problems and challenges!
  - High speed memories (e.g. DDR3, GDDR5)
  - Parallel buses with timimg-critical (accurate) protocols
  - High-speed serial buses (e.g. USB 3)
  - Extensive usage of LVDS interconnections
  - Usage of different signaling standards – reconfigurable IO
  - Growing importance of dynamic defects – delays, crosstalk (signal integrity)
  - Flash programming: size of flash images doubles every 12 months
  - Sometimes ICs need to be again tested after soldering
- BS cannot cope with signaling & speed issues any longer
- Result: the test application paradigm is changing!

Test Access: The Change of Paradigm

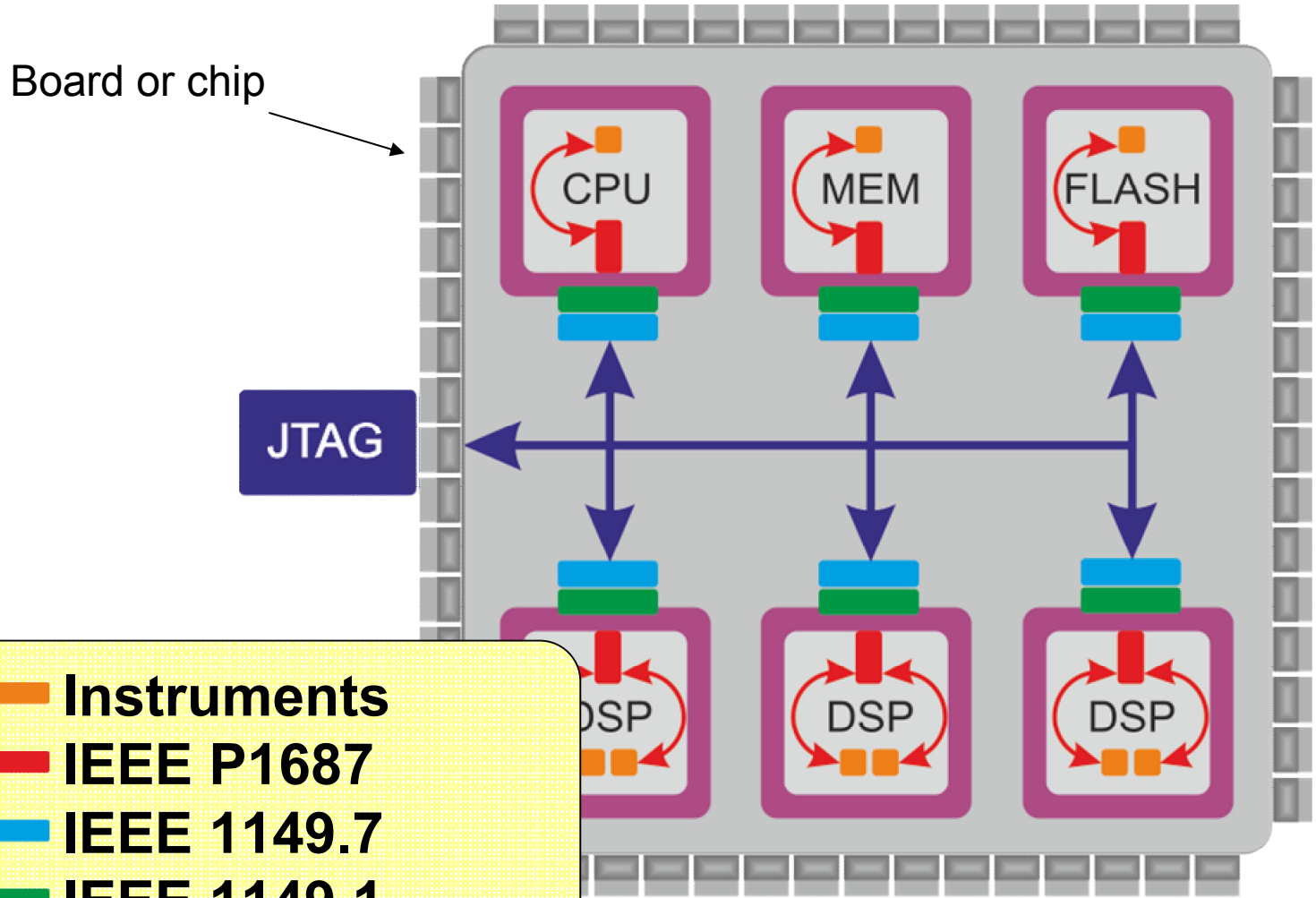
In the near future:

- Boundary scan is no longer a test application method but a **way to communicate** with test application mechanisms
- Test application needs to be done by embedded instruments specifically designed to communicate with a target device/bus or to test/monitor/diagnose specific faults
- Performance of the JTAG-based data transfer mechanism needs to be improved

New Standards and Their Applications

- IEEE 1149.7 – improved flexibility of the JTAG bus by relaxing topology requirements and by addressing resources; potential data throughput improvements
- IEEE P1149.8.1 – improved observability for measurement (from the JTAG standpoint) by implementing a capacitive sensing technology
- IEEE P1149.1-2011 – solves signaling issues on the buses by driver initialization procedures
- IEEE P1687 – introduces the concept of embedded instrumentation for test application, measurement and diagnosis tasks
- Processor emulation standards (e.g. NEXUS) and solutions – converts a MPU into a test instrument

New and Emerging Standards Combined



Overview of IEEE 1149.7

- IEEE Standard 1149.7: IEEE Standard for Reduced-pin and Enhanced-functionality Test Access Port and Boundary Scan Architecture

- Status: Ratified by the IEEE in Dec 2009

The Purpose of 1149.7

The Purpose of 1149.7

- 1149.7 is not a replacement for 1149.1
- 1149.7 uses 1149.1 as its foundation
- 1149.7 provides 1149.1 extensions
- 1149.7 provides 2-pin operating modes
- 1149.7 provides a standard gateway to the pins
- 1149.7 is a complementary superset of the 1149.1

Implementation Ready

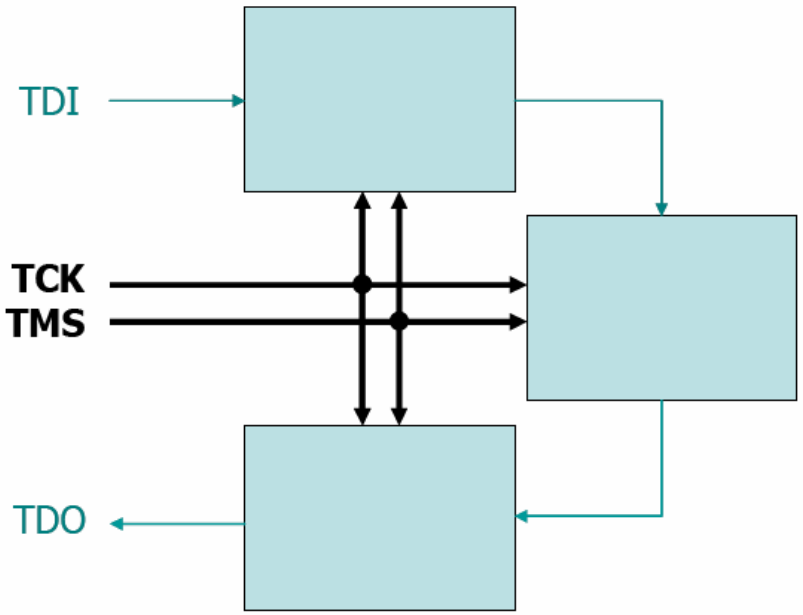
- DTS and TS IP available from **IPeXtreme**
- Verification solutions available from **Globetech**
- Tool support available from major BS tool vendors

Main Benefits of 1149.7

- Power consumption: Test logic power-down
- Performance:
  - Shortened multi-chip scan chains
  - Glue-less star configuration
  - Faster downloads to target
  - Equivalent performance with fewer pins
- Pins: reduce pin usage while adding functions
- Instrumentation: adds a gateway to P1687 instruments
- Flexibility: support of systems-in-packages (SiP), systems-on-chips (SoC), 3D chips.

Compatibility with 1149.1

- The 1149.7 provides for a chip-level 1149.7 Controller that bridges the 1149.1-accessible System Test Logic to the two wires of the chip-level 1149.7
- The chip-level 1149.1 structures are preserved (TAP Controller, chip-level BS register, EXTEST, PRELOAD, and SAMPLE instructions
- Conventional 1149.1 is based on scan operations on test data, hence TMS
- Control extensions are overlaid on *sequences* of TAP Controller states



1149.7: Incremental Capability Classes

IEEE 1149.1 Extensions

- Class T0 – Ensures IEEE Compliance for chips with multiple TAPs
- Class T1 – Adds control functions (e.g. functional reset, power)
- Class T2 – Adds performance features for Series configurations
- Class T3 – Adds Star topology configuration

Advanced Two-Pin Operation

- Class T4 – Adds two pin operation
- Class T5 – Adds instruction/custom pin use to two pin operation

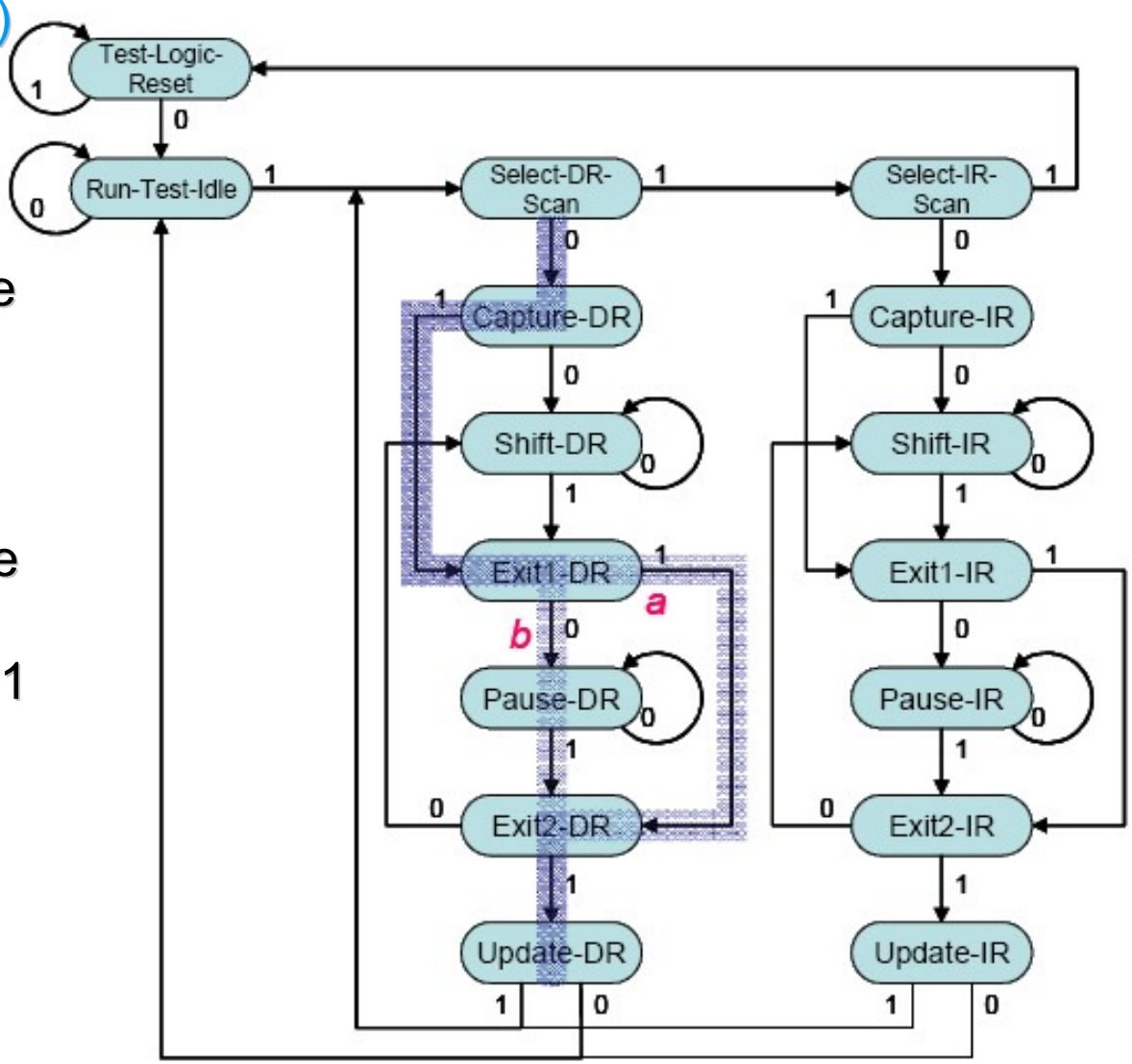
Regardless of which capability class is implemented, a given 1149.7 must implement all of the mandatory features of its own class as well as those of all lower-numbered classes (T0 < T5)

Capability Class T1

Zero-bit DR scan (ZBS)

The extended control mechanism operates without disruption to the 1149.1 TAP state machine.

It uses a particular state sequence, which is based on normal 1149.1 operations, to initiate 1149.7-defined action



Capability Class T1

- Commands are recognized by counting the number of TCK ticks in the Shift-DR (without use of TDI/TDO pins)
- Commands are given in two scans that immediately follow the completion of the non-zero-bit DR scan that locked the ZBS count
- The primary command words are coded in 5 bits (max 31 TCKs)
- All commands include two such parts for a total code length of 10 bits
- T1 provides 4 modes of power management, e.g.:
  - allow power down if TCK stops at logic one for more than 1 ms
  - allow power down if the device is in the Test-Logic-Reset state

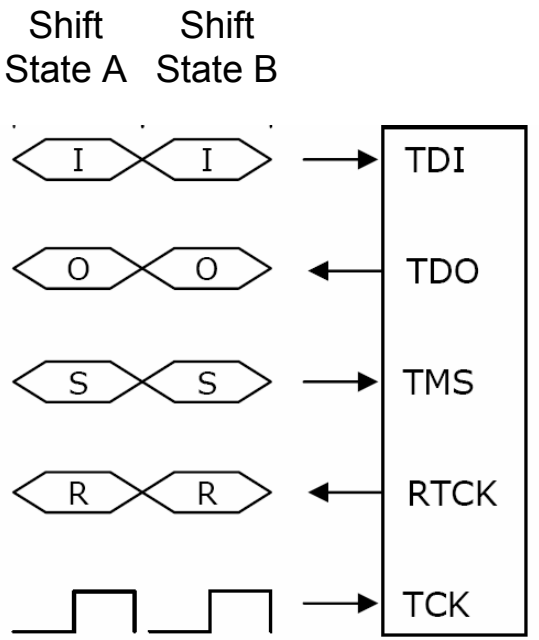
Higher Capability Classes

- Additional classes add scan formats, direct addressability, packetization of scan data (TMS, TDI, and/or TDO information) onto the TMS wire (hence, redesignated TMSC), and finally packetization of non-scan information onto TMSC to provide for transport of background and/ or custom data.

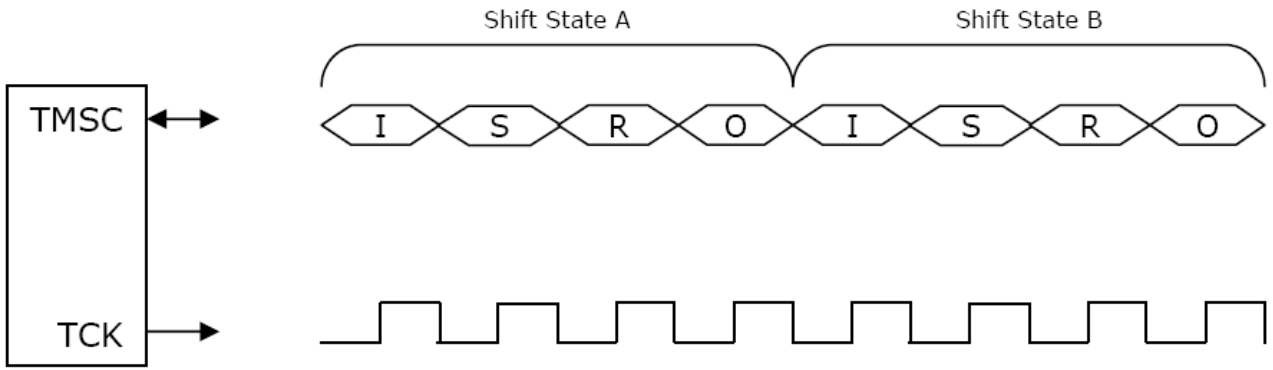
- See more details in the standard!

2-Wire Operation

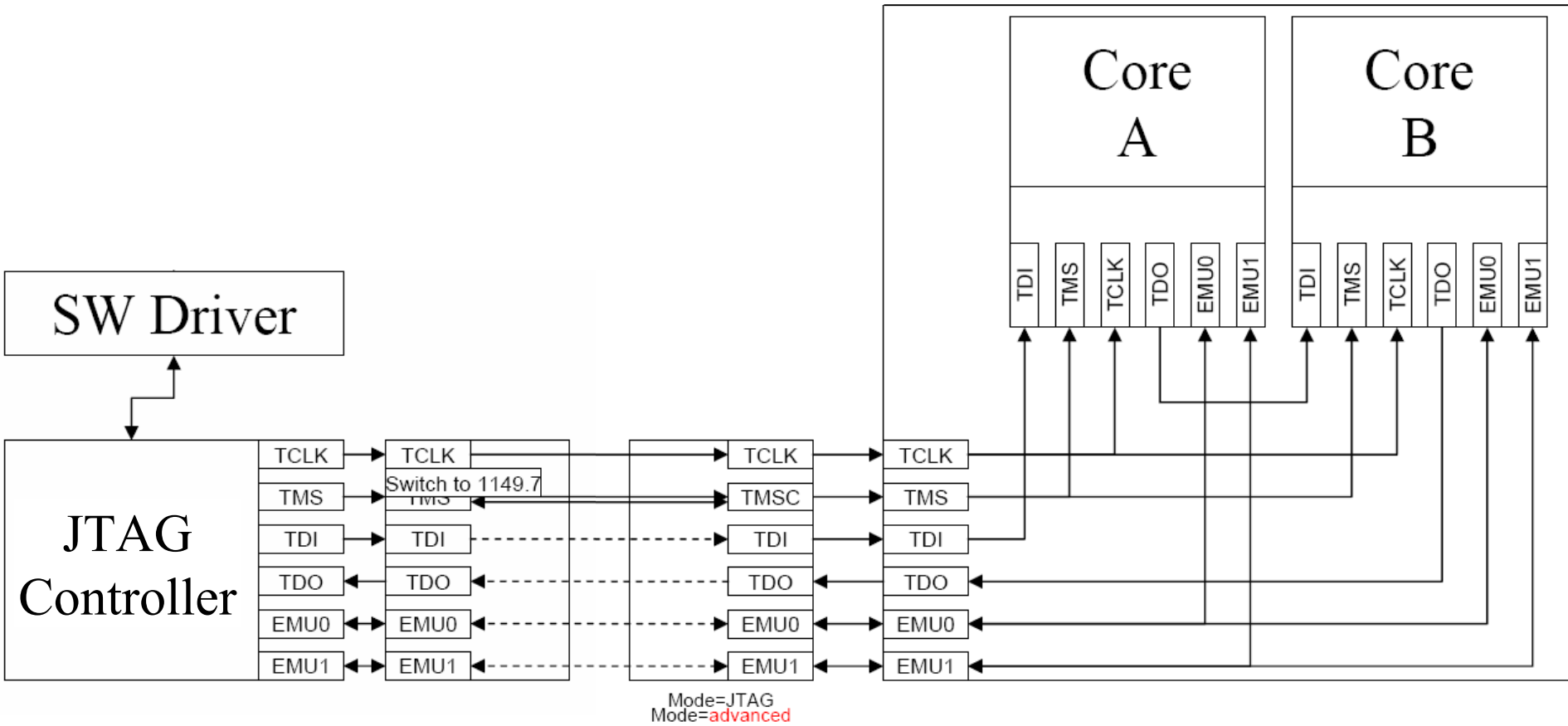
1149.1



1149.7



2-Wire Operation



Overview of IEEE 1149.1-2011

- IEEE Standard 1149.1: IEEE Standard Test Access Port and Boundary Scan Architecture – a new revision

- Status: Draft (activities started late 2009)

The Purpose of 1149.1-2011

- Standardize initialization of complex I/Os prior to test
- Better support and relaxed rules for differential drivers/receivers
- Support for no-connect pins in packages
- Improved support for linkage-ground-power pins
- SAMPLE - request permissions to capture static values on high speed advanced I/O pins
- Clarification on use of TRST

New Features

- INIT_SETUP / INIT_RUN
  - Configure on-chip resources for I/O
- CLAMP_HOLD / CLAMP_RELEASE
  - Hold pins for in-situ on-chip tests
- IC_RESET
  - Reset IC blocks through JTAG
- BSDL for internal JTAG TDR registers
  - For BIST/PLLs/SERDES/ IP blocks
- MNEMONICS for JTAG registers
  - Easy to remember words

Configurable I/O

- The complexity and variation of I/O cells as well as the ICs has greatly increased
- Safe operating voltage ranges of transistors reduced
- I/Os are often configurable for the electrical characteristics such as power levels, drive strength, VIL/VIH, impedance, etc.
- Unused I/O may be configured to be power downed and to not actually be capable of receiving logic values placed on the pin for lower power modes
- In both mission and test modes, I/Os often require configuration before they can be used

Boundary Scan Operation Failures

- I/O cannot correctly drive or receive a logic 1 or 0 until the correct configuration for the given instance is loaded and known
- Mismatched configurations of I/Os on a board could cause a driven logic 1 to be received as a logic 0
- In mission mode, a powered-off I/O analog cell cannot SAMPLE the pin value to the BSR
- Until an Initialization Procedure is completed to program or configure the I/O, none of 1149.X instructions which control or observe the pins can be reliably depended on to correctly operate

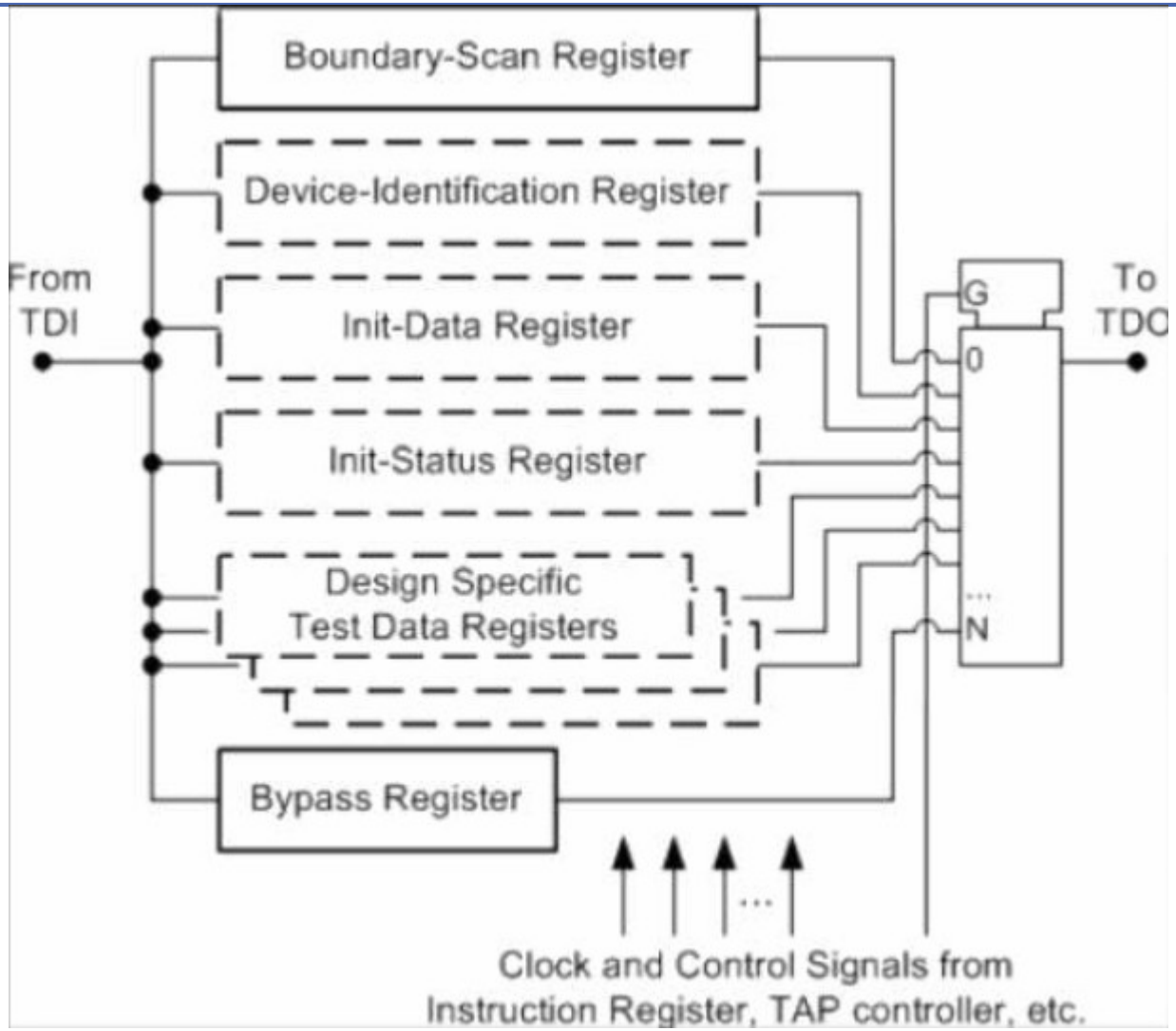
New 1149.1-2011 Instructions

- 2 instructions:
  - INIT_SETUP (optional INIT_DATA TDR)
  - INIT_RUN (optional INIT_STATUS TDR)
  - Run after POR, before EXTEST
  - NOT dependent on RTI TAP state
- BSDL to document the data fields of INIT_DATA) with optional mnemonics for field values, Completion time, and optional expected results (format, content TBD)
- Side file to specify per chip instance initialization data and expected results

BSDL Updates for Initialization

- BSDL will have new Attributes and Keywords for Initialization
- Update `INSTRUCTION_OPCODE` to add INIT_SETUP and INIT_RUN in
- Update `REGISTER_STATUS` to add INIT_DATA and INIT_STATUS
- Create `REGISTER_MNEMONICS` Attribute to describe optional mnemonics for data fields
- Create `REGISTER_FIELDS` to define the subfields of the INIT_DATA or INIT_STATUS register sub-fields

Initialization of Complex I/Os

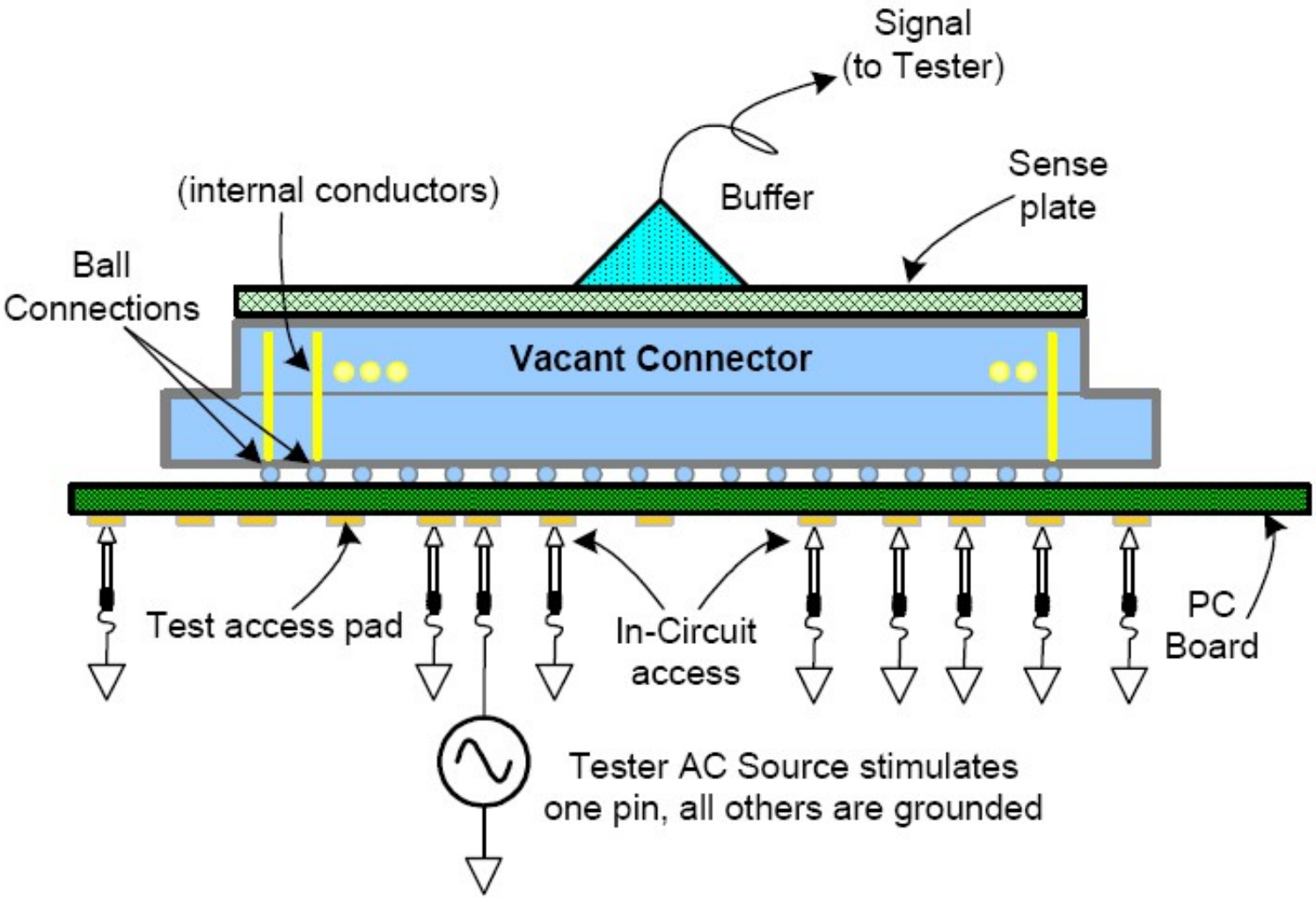


Overview of IEEE P1149.8.1

- IEEE Standard P1149.8.1: IEEE Draft Standard for Boundary-Scan-Based Stimulus of Interconnections to Passive and/or Active Components

- Status: Draft

Principles of Capacitive Sensing



Purpose of the Standard

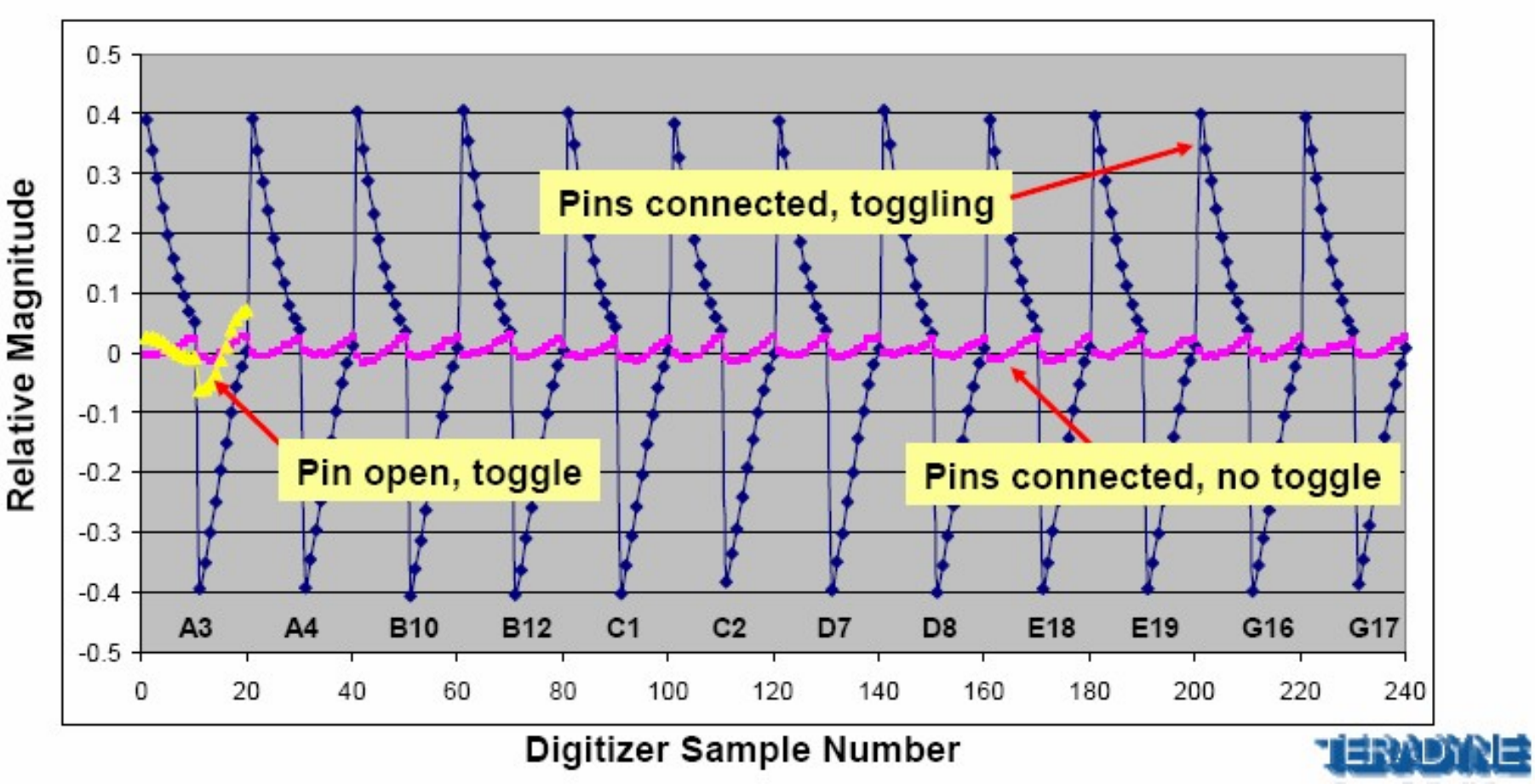
- Use the Boundary Scan infrastructure to deliver an AC stimulus to a single pin or a small number of pins of an IC, while all other signal pins (except TAP pins) “hold” their signals at constant logic 0 or 1

Operation Details

- The toggling takes place during the Run-Test-Idle state
- Toggling only occurs when the SELECTIVE_TOGGLE instruction is active
- The logic value at the output of each boundary scan cell's Update latch must be the logic value that a non-toggling output pin would drive in EXTEST mode.
- The logic value is shifted in using the normal scan-in and update sequence while a PRELOAD or EXTEST instruction is active.
- The logic values shifted in during SELECTIVE_TOGGLE will be mostly logic 0s, with pin toggling enabled by a logic 1.

Fault Detection

From NTF 2009 slides:



Overview of IEEE P1687

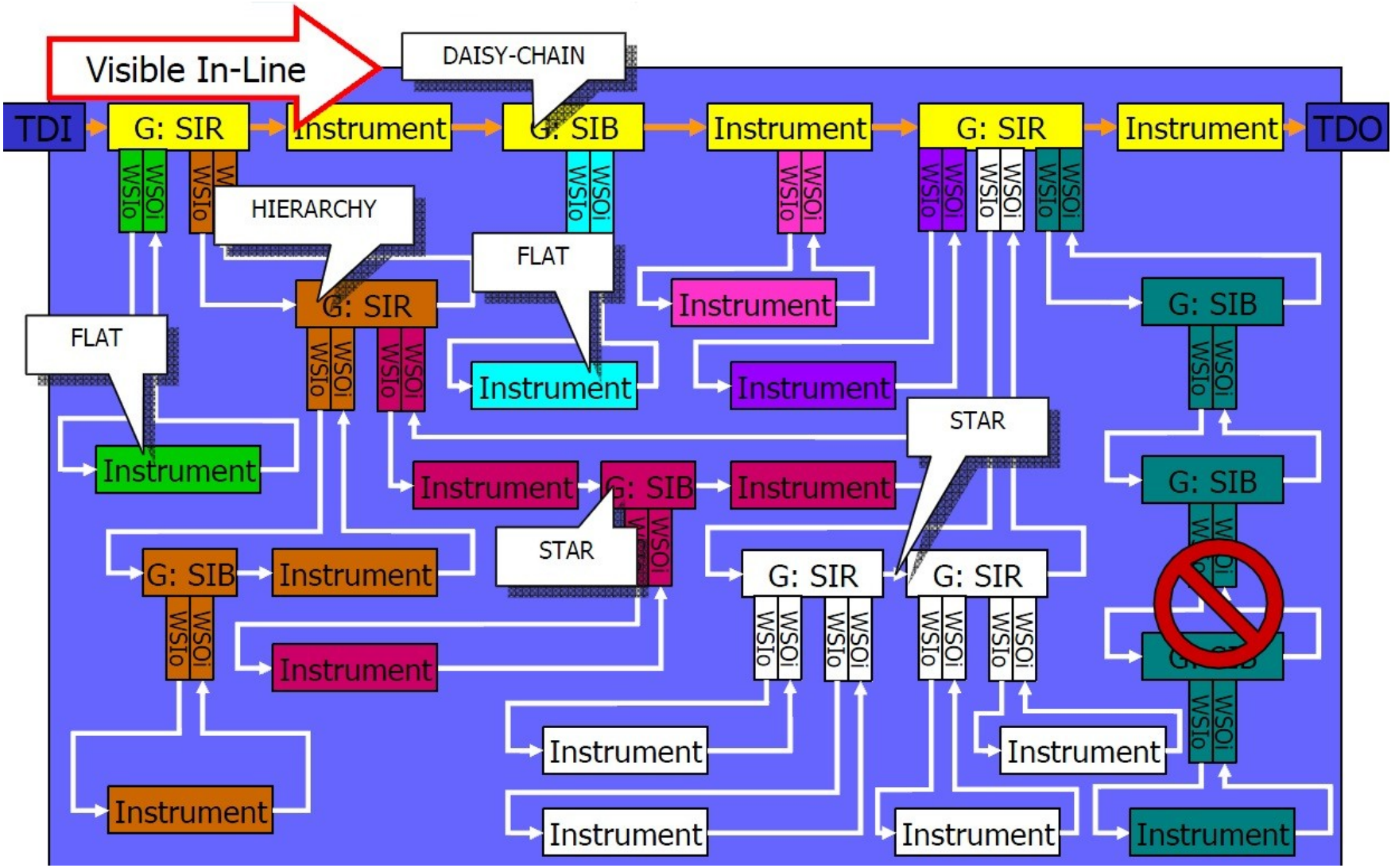
- IEEE Standard P1687: Draft Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device

- Status: Draft (activities started late 2004)

Purpose of the P1687(IJTAG)

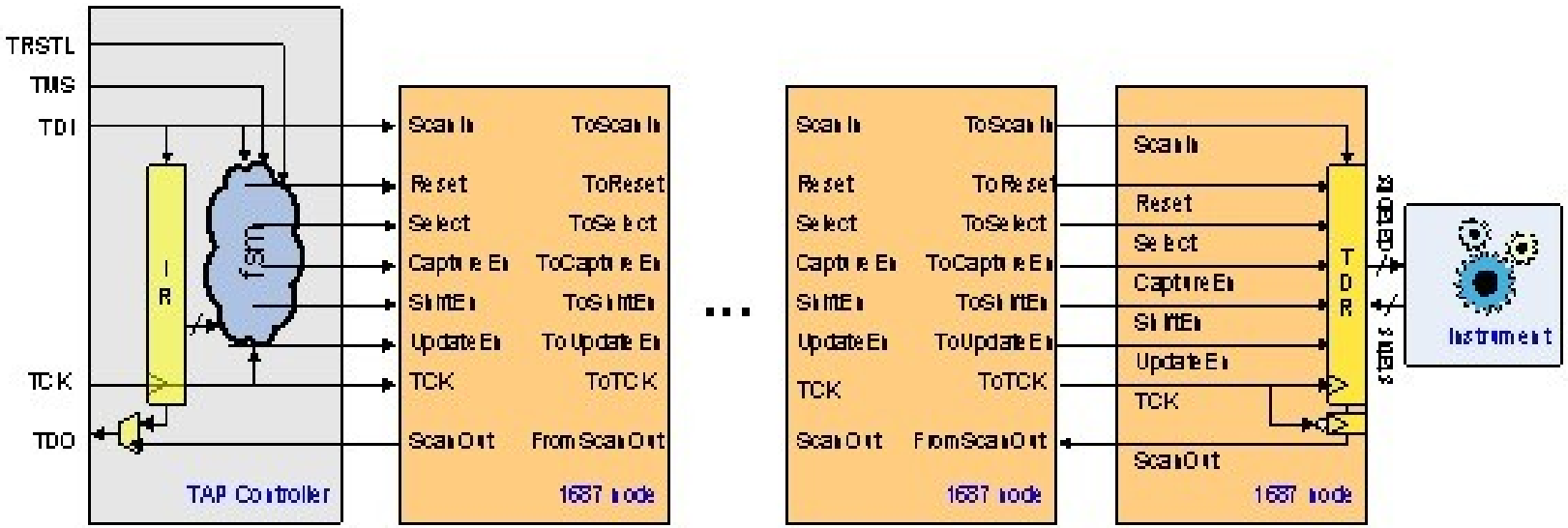
- Introduces standardized on-chip test/debug instrument management;
- Dynamic and efficient instrument connection infrastructure
- Enables good diagnostic/test/debug access
- Standardized instrument connectivity language
- Standardized instrument control language

1687 Debug/Test Instruments



1687 Hardware Architecture

- The basis of the hardware architecture is the network, which connects TAP (and possibly other interfaces) to the instrument:



Instrument Connectivity Language (ICL)

Module (<ModuleName>) {
Attributes {//Miscellaneous constants and attributes , optional
<attributeName> : <attributeValue>;
}
Ports {//Used to list 1687 ports on the module
<PortName> **{…}**
}
Instances {//Used to list instances of other modules in the module
<InstanceName> **{…}**
}
Registers {//Used to list registers in the module
<RegName> **{…}**
}
LogicSignals {//Used to describe muxes and logic driving select ports
<SignalName> : <type> **{…}**
}
}

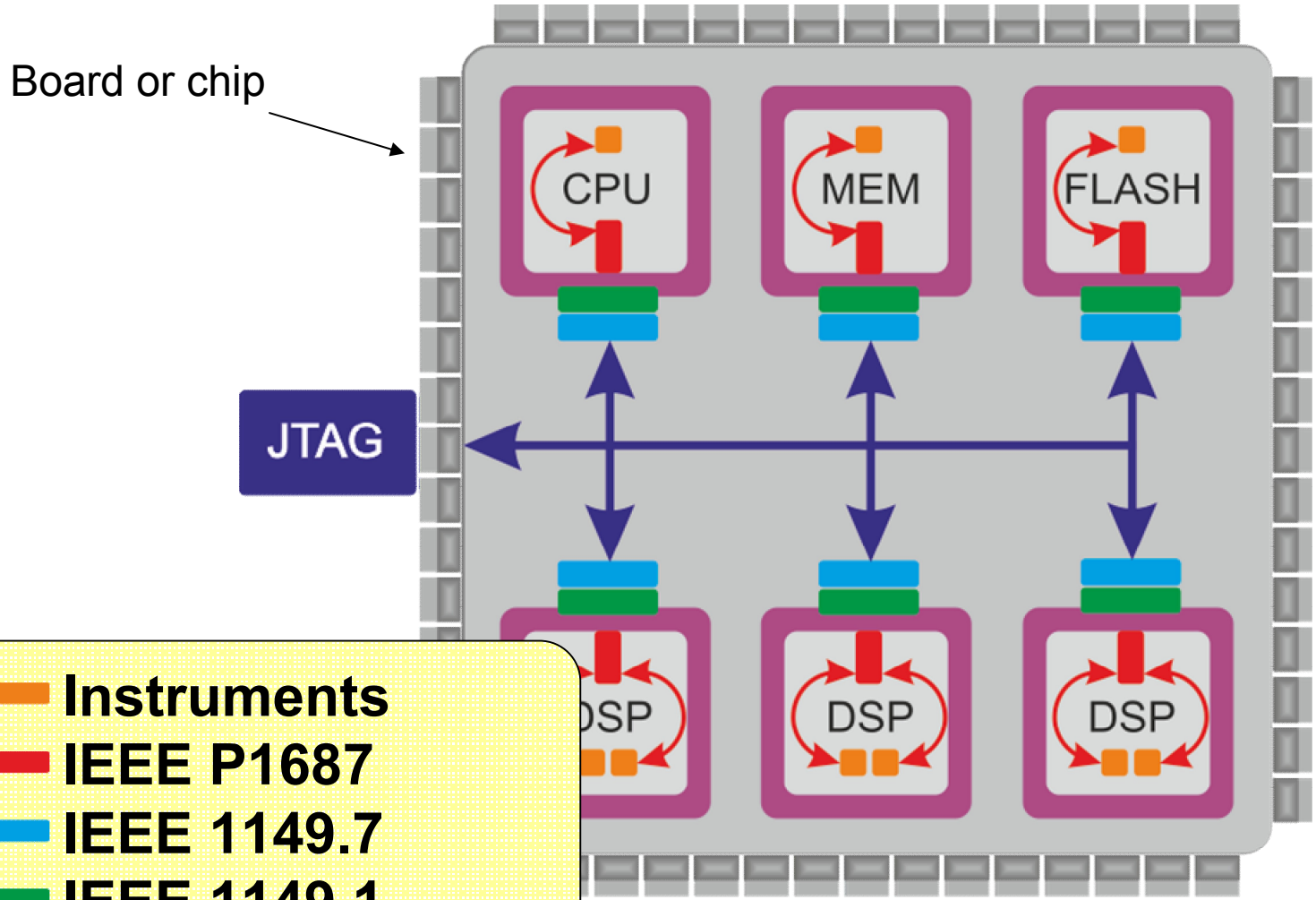
Limitations of BSDL addressed by ICL

- BSDL is flat
  - ICL is hierarchical
- BSDL can only describe a complete TDR once it is connected to a TAP inside a device
  - ICL allows describing each segments in isolation and how they interconnect
    - Localized verification and hand-offs
  - BSDL ends up with on TDR per scan configuration
    - No description of reused segments
- BSDL only supports scan reconfiguration controlled by central IR register
  - ICL supports scan reconfiguration from other TDR bits
- BSDL does not describes logic between Data signals and the TDRs
  - Action commands only possible at the TDR level
    - No retargetting through logic

Procedural Languages

- Procedural Description Language – PDL
  - used for level-0 instructions on instrument level
  - flat and serial language
- Tool Control Language - TCL
  - used for instruments whose functionality requires more complex representation
  - has been selected as the level-1 language of IJTAG

New and Emerging Standards Combined



- Instruments
- IEEE P1687
- IEEE 1149.7
- IEEE 1149.1
- IEEE P1149.1-2011

Conclusions

- Shift in the testing paradigm
- Traditional 1149.1 loses test application functions but retains test data communication functions
- JTAG-based test access and test application methods become very complex
- Growing importance of instrument concept in test application
- Signaling issues and I/O configuration becomes critical