Methods for Access Verification of dRAM devices by Emulation Test

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1. Intro – dRAM Test Problems
2. Emulation Test: top or flop?
3. Available System Solutions
4. Summary and Outlook
Facts on RAM Access Testing by BScan

**Background Information**

- Boundary Scan is well proven for access test of Memories
- Access to all Memory signals from Boundary Scan side needed
- ATPG Tools enabling predictive test coverage calculation
- Automated Pin Failure Diagnostics for static detectable faults
- Use of special Library Models to describe Memory access behaviour
- RAM banks can typically be tested on the base of individual chip activation
Fault Coverage trends via IEEE 1149.1

Average real world BScan Fault coverage Quality for Memory Access

Situation

Fault coverage for Memory Access on modern boards via IEEE1149.1 has been declining continuously for several years. This is caused by use of modern DRAM’s.
Searching for answers...

**Current Test Problems**

- DRAM devices getting continuously higher data rates (DDR2, DDR3...)
- Routing of DDR signals during layout is critical to avoid skews (Design Errors)
- Boundary Scan is too slow to keep the necessary vector rate
- Some processors don’t have BScan on the Memory Bus pins anymore
- Missing access to all Memory signals or non-controllable clocks
- New Standard IEEE 1581 could solve the problem but is not available yet
Some thoughts ...

Conclusions

- BScan test becomes difficult due to the increased speed of the memory chips
- Key challenge is to keep a deep test coverage also for high dynamic structures
- Features like predictive fault coverage, ATPG and pin level diagnostics are needed
Where is the future?

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BScan Test versus Emulation Test

**Boundary Scan Test**

- **Boundary Scan TAP**
  - TAP Controller
    - Instruction Register
    - Standard Data Registers
  - BScan Register
  - Pin Interface

  - Static pin electronics
  - BScan cells define vectors
  - Serially controlled pin interface
  - Scalable number of pins
  - Arbitrary static signal timing
  - Arbitrary vector definition per pin

**JTAG Emulation Test**

- **JTAG Emulation TAP**
  - TAP Controller
    - Instruction Register
    - Standard Data Registers
    - Emulation Registers
  - I/O Controller (µP Core)
    - Pin Interface (System Bus)

  - Dynamic pin electronics
  - µP defines vectors
  - Parallel controlled pin interface
  - Fixed number of pins
  - Rigid dynamic signal timing
  - just Address / Data bus controllable
Interconnection of µP Core and DRAM

**Pro’s**

- Test Access ready by design
- No special DfT rules necessary
- Free running clocks: no issue
- Real Time functional Test
- Advanced structural emulation Test methods possible

**Control Hardware**

**Chip Level**

- µP Core
- System Bus I/F
- On-Chip Resources
  - Embedded Flash
  - Complex Bus I/F
  - Legacy Bus I/F
  - Legacy I/O Ports

**Board Level**

- External Bus Devices
  - Flash Components
  - SRAM / DRAM
  - Peripheral I/O Ports
  - Peripheral Bus I/F
  - Aux Resources

**JTAG TAP**
New methods by emerging standards

IEEE P1687

IEEE1687 controlled Test Instrument (IP)

Address

Data

Control

DRAM

IEEE1149.1 / IEEE1687 Access

Access Verification of DRAM by embedded Test Instrumentation compliant to IEEE1687

IEEE P1581

IEEE1581 compliant Device

Address

Data

Control

DRAM

IEEE1149.1 Access

Access Verification of DRAM by Boundary Scan in conjunction with IEEE1581 activation
Progress with handicaps ...

Conclusions

- Emulation Test offers the needed test speed but has limits driving control signal
- Achievable Fault coverage is identical to BScan Test but diagnostics quality is lower
- Need for System solutions to support advanced Emulation Test and emerging standards
One Target – Different ways

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Solution #1: Special coded Test Routine

Test Routine Development with native s/w Tool chain

Executable

Download into Flash and Program Execution

Debugging of s/w and h/w via Emulator

JTAG Emulator

Chip Level

μP Core

On-Chip Resources

- Embedded Flash

- Complex Bus I/F

- Legacy Bus I/F

- Legacy I/O Ports

System Bus I/F

External Bus Devices

- Flash Components

- SRAM / DRAM

- Peripheral I/O Ports

- Peripheral Bus I/F

- Aux Resources

Board Level

Dec 1-2, 2009, Stockholm, Sweden
Solution #2: Configurable Test Routine

- JTAG/ BScan Hardware
- Configuration of standard Test IP by parameters
- Executable
- Program Execution using just the µP Core
- GO/NOGO and Failed Vector level Diagnostics
- µP Core
- On-Chip Resources
  - Embedded Flash
  - Complex Bus I/F
  - Legacy Bus I/F
  - Legacy I/O Ports
- System Bus I/F
- External Bus Devices
  - Flash Components
  - SRAM / DRAM
  - Peripheral I/O Ports
  - Peripheral Bus I/F
  - Aux Resources
- Board Level
- Chip Level
- JTAG TAP
Solution #3: Automated Testing (ATPG)

- JTAG/ BScan Hardware
- ATPG for structural Test Vector Generation
- Test Program
- Program Execution using just the µP Core
- Pin Failure Diagnostics by system software
## Comparison of System Solutions

<table>
<thead>
<tr>
<th>Features</th>
<th>Special coded Test Routine</th>
<th>Configured Test Routine</th>
<th>ATPG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manually s/w Source coding</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Use of native MCU tool chain</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Automated Vector Generation</td>
<td>no</td>
<td>Semi automated</td>
<td>yes</td>
</tr>
<tr>
<td>Predictive Fault coverage calculation</td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>True Interlaced BScan/Emulation operations</td>
<td>no</td>
<td>no</td>
<td>possible</td>
</tr>
<tr>
<td>Unified BScan/Emulation test commands</td>
<td>no</td>
<td>no</td>
<td>possible</td>
</tr>
<tr>
<td>Flash firmware programming needed</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Total Programming and Test execution time</td>
<td>High</td>
<td>low</td>
<td>low</td>
</tr>
<tr>
<td>Unified hardware for BScan and Emulation</td>
<td>no</td>
<td>possible</td>
<td>yes</td>
</tr>
<tr>
<td>Pin Level Diagnostics</td>
<td>possible</td>
<td>Vector level</td>
<td>yes</td>
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<tr>
<td>Truth Table visualization of test execution</td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
</tbody>
</table>
Technology Status

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Quo Vadis Memory Access Test...

Conclusions and forecast

BScan by IEEE1149.1 is not able to cover memory access tests for high speed dRAM

Emulation Test is an excellent problem solution. Key is the used system architecture.

New standards like IEEE1581 and IEEE1687 will close the test coverage gap further
More information...

Further readings and References

[1] Jan Heiber – Boundary Scan versus Emulation Test
Proceedings of the Nordic Test Forum 2008, Tallinn

Boundary Scan and JTAG Emulation for advanced
structural test and diagnostics
White Paper, GOEPEL electronics, 2009

Test Protocol and architecture

Embedded within a Semiconductor Device.
Thank you for your attention.

Any Questions?

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