Creating a Single, Seamless, End-to-End Test Process

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The New DFT

Delayed Flights to Tallinn
If we knew what it was we were doing, it would not be called research, would it?

Albert Einstein
Board?
Or Chip?
Traditional System?
2nd Workshop on

Diagnostic Services in Network-on-Chips

— Test, Debug, and On-Line Monitoring —

Monday, June 9, 2008
2D Mesh Interconnect

S. Vangal et al., “A 5.1GHz 0.34mm² router for NoC applications”, VLSI Circuits Symp. 2007

- 10×8 2D mesh network
- 2nd generation 100GB/s Router
- 5 port, fully non-blocking router
  - 6th port added for 3D support
- Two 39b unidirectional links
- Phase-tolerant communication
- Source directed, worm hole routing
- Two virtual lanes
- 5GHz operation @1.2V
- 320GB/s LIS section B/W
- 6 cycle latency (1.2ns)/hop
- On/off flow control

High bandwidth, Low-latency fabric
What Differentiates Chip from Board from System?

- Architecture/Functionality?
- Interfaces/Interconnects?
- Test/DFT?
- Manufacturer?
- BOM hierarchy?
Today’s Chip(?) Complexity

Doppler ASIC Architecture Specification

Reviewers

<table>
<thead>
<tr>
<th>Department</th>
<th>Name/Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Development Engineering</td>
<td></td>
</tr>
</tbody>
</table>

Modification History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Originator</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>01/31/2007</td>
<td>Surendra Anubolu</td>
<td>Initial Rev</td>
</tr>
<tr>
<td>0.2</td>
<td>02/05/2007</td>
<td>Surendra Anubolu</td>
<td>Added External Interface section</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Moved to channelized interface</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Move RWE out of FC</td>
</tr>
<tr>
<td>0.3</td>
<td>02/18/2007</td>
<td>Surendra Anubolu</td>
<td>Added 4K usage section</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Added TED block to Recirculation</td>
</tr>
</tbody>
</table>
R2D2 SiP Module Application
High Density Switching Line Card
Base Board

Four R2D2 SiP Modules
Daughter Card with Four SiP Modules
Combined Line Card
Integrating Line Card into Switch
Integrating Switches into the Network
Most Critical DFT Decisions

Moore’s Law Accelerated

Moore’s Law$^3$
Global Supply Chain Management at Cisco

Team
- ~9,000 employees
- 50+ locations/17 countries
- 10 functional groups

Main Locations
San Jose, CA; Amsterdam, NE; Atlanta, GA; Austin, TX; Boxborough, MA; Hong Kong, PRC; Irvine, CA; Juarez, Mexico; Penang, Malaysia; RTP, NC

By the Numbers
- >1,000 suppliers
- 150,000 new serial numbers generated per day
- 2.5 million test records processed per day
- 95% of manufacturing is outsourced

*Includes Scientific Atlanta and Linksys
Digression – Stanford Gene Folding
Digression – Ubiquitous Computing
Digression – The Next Big Router??
How do We Handle the “Hierarchical System”

- DFT in the right place at the right time
- Everybody speaks the same language
- Data, Data, Data
Detecting the problem is easy – finding the problem is the problem

- Partition the design into “testable” blocks
- Embed test structures:
  - To ensure high coverage in the block
  - To test all interfaces to the block
  - Must be usable at ALL levels of the hierarchy (ie. Everyone needs to speak the same language)
Most Critical DFT Decisions
Two methods to access built-in test features:
1. JTAG for board test
2. CPU to all ASICs for on-line/off-line system test
Speaking the Same Language - IJTAG

Active P1687 (IJTAG) Working Group

- Chair: Ken Posse (Avago)
- Vice Chair: Al Crouch (Asset-InterTech)
- Editor: Jeff Rearick (AMD)
- Web Master: Michael Laisne’ (Qualcomm)

Current Working Group Members:

- Jason Doege (AMD); Mike Ricchetti (ATI); Srinivas Patel, Mike Wiznerowicz (Intel);
- Bill Eklow, Hongshin Jun, Ted Eaton (Cisco);
- Songlin Zhuo (Qualcomm); Pradipta Ghosh (Broadcom);
- Hugh Wallace, Rick Nygard, Richard Dugan (Agilent); Scott Hartranft (Tektronix)
- Thomas Rinderknecht, Paul Reuter (Mentor); J.F. Cote (LogicVision);
- Rohit Kapur (Synopsys) – 1450.6 CTL Liason; Ed Malloy (Cadence);
- Bill Tuthill (Intellitech); Stylianos Diamantidis (GlobeTech); John Potter (Asset-InterTech);
- Harrison Miles, Andrew Levy (Corelis); Heiko Ehrenberg (Goepel);
- Brad Van Treuren, Michele Portolan, Suresh Goyal (Alcatel-Lucent); Thai-Minh Nguyen (LSI)

A Camel is a Horse designed by committee…
The Board World Today

**Basic Goal of Board Test:**

To verify that the correct chips are in systems and they also are in the correct spots; the orientation of chips; and the environment margins; completeness of interconnect; connectivity needs to be understood to deliver vectors to the chips.

There is a need for a simple linear indexing system to map chips.

Chips are delivered with BSDL Files to describe JTAG features.

Chip instructions are not required to be mapped identically.

Chip TDI-TDO connections create the access map and are not required to be identical on all chips.

BSDL Description

BSDL is sufficient for chip JTAG description and connection.

Chip JTAG Instructions Extest, Sample, Preload, HighZ, etc. allow pins to be interconnect tested.

1149.1 (JTAG) is used on board designs to conduct board test because it can be used without external probing equipment.

Connectivity needs to be understood to deliver vectors to the chips.

Chips need to be described in terms of pins and boundary scan cells.

Let’s look inside
In the world of electronics, it's crucial to understand how to connect and test instruments within a chip. The BSDL (Behavioral Schematic Description Language) is insufficient for instrument description and hierarchy. Instruments need to be described in terms of purpose and attributes.

**Inside-the-Chip Instrument Map**

The goal is to deliver static drive signals and to extract static status signals from a leaf instrument node using a JTAG-operated open access interface. Connectivity needs to be understood to deliver vectors to the instruments.

Groupings may be separate IP cores or macros, and Scan Compression can be separate. Instruments may be fault-tolerant, using multi-input connections to minimize broken scan path risk.

Gateways enable hierarchical connections that allow architectures driven by tradeoffs. Instruments are most likely delivered “raw” with signal I/Fs.

**BSDL (Behavioral Schematic Description Language)**

Gateways can be viewed as distributed instructions that represent “bypass” bits to bypass instruments. There is a need for an adjustable indexing system to allow mapping.

In the chip, there are zones: 1149.1 Zone and 1687 Zone. The BSDL is insufficient for instrument description and hierarchy. Instruments need to be described in terms of purpose and attributes.

**Core Debug Unit**

Gateways may be daisy-chained to create hier-levels. There is a need for an adjustable indexing system to allow mapping.

**Bus Configuration**

Connectivity needs to be understood to deliver vectors to the instruments.
Warning! This stuff is changing as we speak... meetings are being held... skids are being greased... engineers are skulking around in dark corners (uh, different ones than they usually hang around)... crayons are being brought to bear... waitresses are being short-tipped for all day meetings in restaurants...
ATE vs System Environment

- High coverage test program
- Low noise loadboard design
- Stable temperature
- Very accurate power supplies

- Functional test (Coverage???)
- Complex system board design
- Multiple chips interfacing to each other
- Noisy environment

SAME voltage, temperature, frequency?
Diagnosis of Board ASIC Fails at System Test from a major High Tech Company

Diags 9%  
CM Process Enhancement 11%  
Design 13%  
Packaging 2%  
Supplier Test Enhancement 66%
Internal Clock Control – Transition test

![Graph showing internal clock control transition test results]

- 6.625ns
- 5.5ns
- 5.6ns
- 6.776ns
Fixing defects at the component supplier

DATA is KEY
Usage by Mnth/CM
DPPM by Mnth/CM
Improved Data: Fail Symptom

‘Unknown’
Scan Imager Project – Lbist deployment

Any ATE

Asset / PC-Scan

Diagnostics

Scan Imager
Scan Imager Logical Plot

“Scan Chain” view (zoom in)

Fail Datalog

Sliders

Hierarchy/Block
Scan Imager Physical Plot

Zoom view

Datalog

Full View
How ECID helps catch Iddq Outliers

- Why ECID is so useful:
  - ASICs failed system test
- Key Analysis Tools
  - ECID Regionality Analysis
    - Parametric characterization of data for anomalies
- Actions Taken
  - Parametric test limits tightened to capture RMA, lower DPPM
Collaboration in a Virtual Supply Chain

- Component Suppliers
- EMS Partners
- System Integrator
- Customer

Quality Data Infrastructure

Cisco
IMAGINE...

- Everyone has instant availability for any key attribute
- Open information exchange between every supplier
- Every Failure Analysis results in permanent prevention
- Customers never having to return hardware